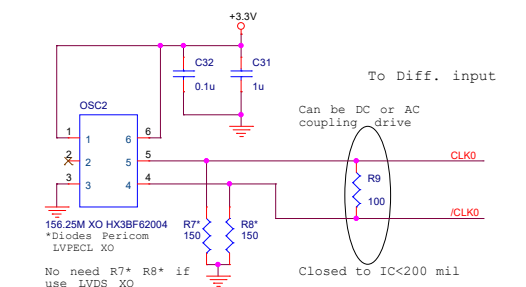
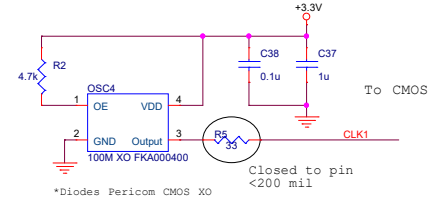
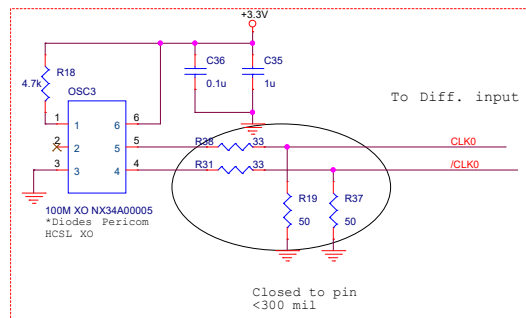
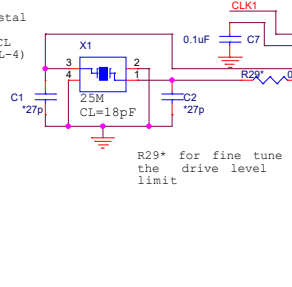


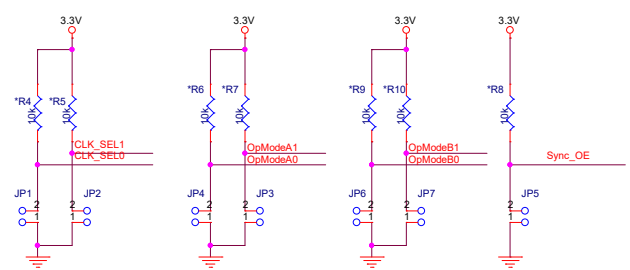
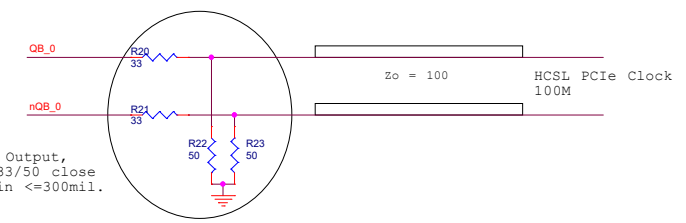
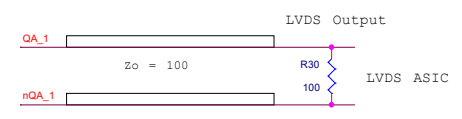
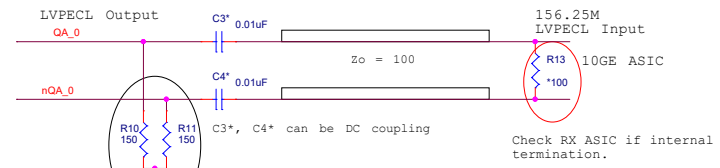
VDDO are output supply, design VDD = or > VDDO



Select CL=18pF Crystal can have load cap. Cl=C2=27pF, other CL crystal Cl=C2=2x(CL-4)



Device setting:
Input CLK_SEL[1,0]:
Set CLK_SEL0 logic in R4/JP1, CLK_SEL1 in R5/JP2
0 0 IN0
0 1 IN1
1 X XTAL
OPMODEA/B[1,0]:
Set OPMODEA0 logic in R6/JP4, OPMODEA1 in R7/JP3, OPMODEB0 logic in R9/JP6, OPMODEB1 in R10/JP7
0 0 LVPECL
0 1 LVDS
1 0 HCSL
1 1 Hi-Z
Sync_OE:
Set Sync_OE logic in R8/JP5
Set "0" for Ref Out disabled
Set "1" for Ref Out enabled



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- App Note:
1. Select IN0, IN1 or XTAL as input ;
 - 2.1 Each VDD pin needs 0.1u +1uF decoupling close to pin. (e.g.: VDD, VDDO, ...etc)
 - 2.2 VDD use small R=1~2 ohm or FB(ferrite bead)+C=10uF filtering for better DC/DC ripple noise rejection
 3. LVPECL Output: Place 150ohm pull-down in comp. side close to pin <=300mil.
 - HCSL Output: Place serial 33 ohm and 50ohm pull-down in comp. side close to pin <=300mil.
 4. Suggest to use DC coupling in LVPECL/LVDS drive input clock with 100ohm cross at input pins <200mil; HCSL drive input clock without 100 ohm cross at input pins.
 5. when in AC input drive either just use 100ohm cross to bias balance